A Design of 80 GHz Cascode LNA for W-Band Level Sensing System

Chung Geun Jang
ICT Device & Packaging Research Center
KETI(Korea Electronics Technology Institute)
Sungnam-si, Korea
cgjang@keti.re.kr

Kj-Jin Kim
ICT Device & Packaging Research Center
KETI(Korea Electronics Technology Institute)
Sungnam -si, Korea
sergeant@keti.re.kr

Kwang-Ho Ahn
ICT Device & Packaging Research Center
KETI(Korea Electronics Technology Institute)
Sungnam -si, Korea
khajoh@keti.re.kr

Soo-Chang Chae
ICT Device & Packaging Research Center
KETI(Korea Electronics Technology Institute)
Sungnam -si, Korea
sc.chae@keti.re.kr

***Abstract*— In this paper, an 80 GHz two-stage Cascode low noise amplifier for a W-Band level sensing system was designed using the CMOS 65nm process.The designed LNA has a two-stage Cascode amplification stage structure, and parallel and series resistor inductors were applied to remove the parasitic capacitance of the Cascode device.Two techniques are effective in reducing Cascode NF. The gain of the designed LNA is 14.6-17.9 dB, NF 4.4-4.6 dB at 77-81 GHz, and Op1 dB is 2.77 dBm.In the same band, the input/output reflection coefficient is -10 dB and consumes 23 mW of DC power in a 1.2 v supply.**

Keywords—LNA,Radar System,FMCW,CMOS

I. INTRODUCTION

Recently, a level sensor system using millimeter wave FMCW radar has been developed. Millimeter wave FMCW radar can perform better in bad weather environments than laser or infrared systems.

However, due to the nature of the system that processes transmission/reception signals at the same time, if there is insufficient isolation between transmission/reception paths in the millimeter wave radar system, the strong signal and noise of the transmission path are coupled with the reception path, and the low noise amplifier operates in the saturated area.

In addition, signals reflected at close range have large power and low IF frequency, causing difficulty in signal processing These problems are factors that make the system require high sensitivity and linearity.

To solve this problem, this paper presents a low noise amplifier design in the W-Band band with low noise index and high linearity.

II. A DESIGN OF 80 GHZ CASCODE LNA

In this paper, the Cascode LNA design technique was designed by applying the power constrained simple noise and input matching (PCSNIM) method that satisfies input matching and noise matching at the same time while maintaining constant power consumption. Implementing a small Ls value by adding Cex between Gate-Sources to a general Cascode structure reduces NFmin. and improves NF characteristics.

Fig. 2. Cex and Ls of Zs and Zin in the small signal equivalent circuit were selected in the same way, and 50 ohm matching was designed using the matching circuit inductor Lg so that the imaginary components of Zs and Zin were offset.

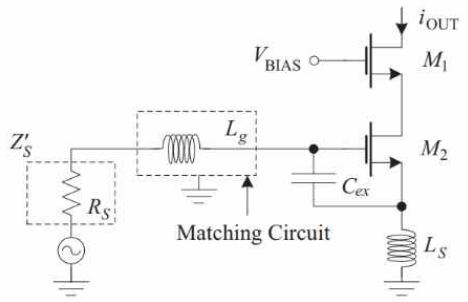

FIGURE 1. CASCODE LNA TOPOLOGY WITH PCSNIM

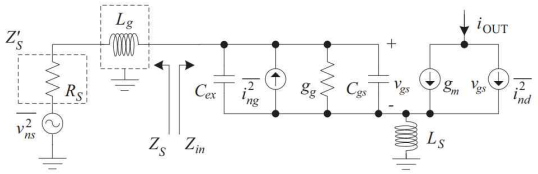

FIGURE 2. SMALL SIGNAL EQUIVALENT CIRCUIT [PCSNIM]

The input impedance of the small signal equivalent circuit in Figure 2 is shown in Equation [1].

$$Z_{in} = \frac{g_m L_s}{C_t} + sL_t + \frac{1}{sC_t};C_t = C_{ex} + C_{gs}\,,\; L_s = L_g + L_s \qquad [1]$$

The input impedance is equal to the source impedance at the operating frequency of Equation [2]

$$w_0 = \frac{1}{\sqrt{L_t C_t}} \qquad [2]$$

The Q-factor of the input matching circuit is as shown in Equation [3].

$$Q = \frac{1}{(R_s + g_m \frac{L_s}{C_t}) w_0 C_t} = \frac{1}{2R_s w_0 C_t} \qquad [3]$$

In a small-signal equivalent circuit, if Equation [3] is applied to the Noise parameter, it is shown in Equations [4] and [5].

$$F = 1 + \frac{\beta'(Q^2 + \frac{1}{4})(Q \cdot 2\omega_0 R_s C_{gs})^2 + \frac{\gamma'}{4}}{R_s Q^2 g_m} \qquad [4]$$

$$F_{min} = 1 + \frac{1}{Q} \cdot 4\beta'^{1/4}(\frac{\gamma'}{12})\sqrt{\frac{2\omega_0}{3\mu_{eff} R_s I_{ds}}}\, L \qquad [5]$$

In addition, CS nMOS and CG nMOS are configured in the Cascode structure, resulting in a significant increase in NF due to the parasitic capacitance of the Cascode node. [Figure 3.]

The total parasitic capacitance between Cascode nodes is as shown in Equation [6], and was designed by applying a series/parallel inductor to remove this parasitic component.

$$C_p = C_{p1} + C_{p2} \qquad [6]$$

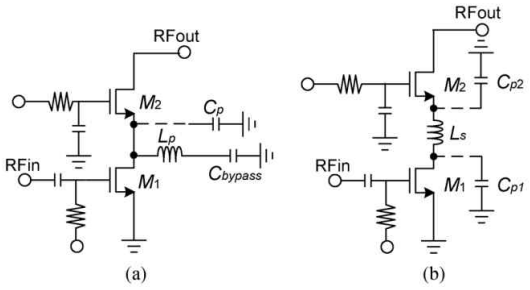

FIGURE 3. SERIES AND PARALLEL RESONANT INDUCTORS (CASCODE DEVICE)

III. MEASUREMENT RESULT

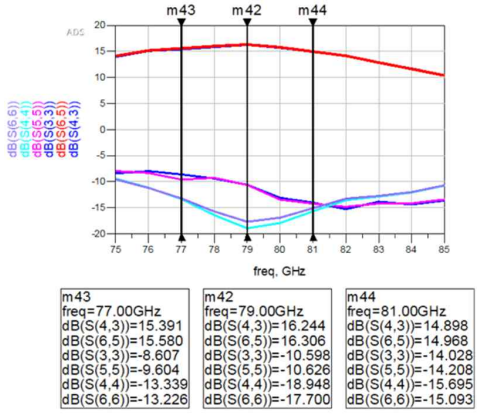

FIGURE 4. LNA S-PARAMETER MEASUREMENT RESULTS

This is the result of the LNA S-parameter measurement, and the results of 14.89 to 16.24 dB for gain and -18.9 to -8.6 dB for reflection coefficient in the frequency band 77 to 81 GHz were confirmed.

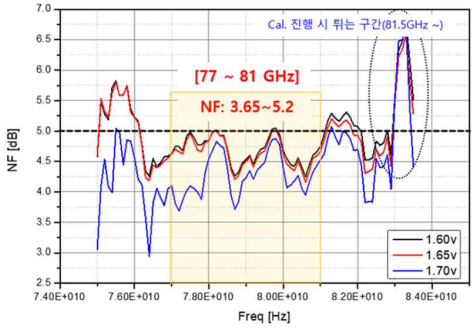

FIGURE 5. LNA NF (NOISE FIGURE) MEASUREMENT RESULTS

This is the result of LNA noise feature measurement, and NF 3.65~5.2 dB was confirmed at 77~81 GHz frequency band.

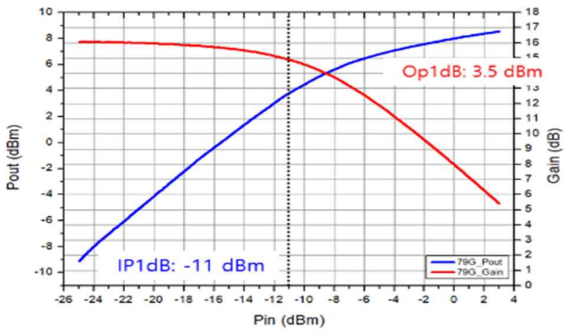

FIGURE 6. LNA P1DB MEASUREMENT RESULTS

This is the result of LNA P1dB (linear formation) measurement, and P1dBm at frequency band 77 to 81 GHz was confirmed as -11dBm.

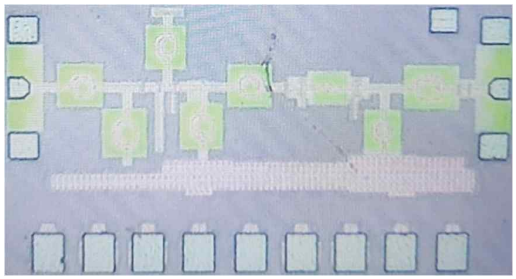

FIGURE 7. LNA IP (850UM × 450UM)

LNA IP Size is 850um × 450um.

IV. CONCLUSION

In this paper, a two-stage Cascode LNA for a W-Band level sensing system using the CMOS 65-nm process was designed. The designed LNA has a two-stage Cascode PCSNIM amplification stage structure, and was designed by applying parallel and series resistor inductors to remove parasitic capacitance of the Cascode Device.

The gain of the designed LNA is 14.89-16.24 dB at 77-81 GHz, NF 3.65-5.2 dB, and IP1 dB is -11 dBm. In the same band, the input/output reflection coefficient is -8.9 dB or less, and DC power of 23 mW is consumed in a 1.2 v supply power supply.

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