A Design of High Resolution ADC-Assisted Gated-Ring Oscillator TDC with Digital Calibration

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***Abstract*— This paper introduces an ADC-Assisted Gated-Ring Oscillator (GRO) Time-to-Digital Converter (TDC) structure with constant and high resolution through digital calibration. This circuit consists of a general GRO based on a multi-path delay cell, a resistive-interpolated Flash ADC to improve resolution. Encoder includes averaging function, and digital calibration. Resolution can be improved three times by utilizing the resistive-interpolated Flash ADC, resulting in a resolution of 4 ps. Additionally, the averaging function can increase the actual output resolution by 8 times, then the final resolution of this TDC can be 0.5 ps. A constant resolution can be secured in all corner cases through digital calibration.**

Keywords—Time-to-Digital Converter, GRO, ADC-Assisted, High Resolution, Constant Resolution

I. INTRODUCTION

A general GRO TDC can cover a wide input range, but it is difficult to have a high resolution depending on the process, and the resolution change is very large depending on the PVT variation. High resolution is essential to be applied to various applications such as ADPLL. It should also be insensitive to PVT variation to keep the entire system stable. For example, if the resolution of the TDC used in ADPLL varies greatly with PVT variation, the loop characteristics will also vary significantly.

To solve the above problem, this paper introduces a GRO TDC that can have a high and constant resolution. High resolution is implemented by using multi-path delay cells [1] , [2], ADC-Assisted topology [3], [4], and averaging. In addition, digital calibration allows the GRO TDC final output to have a constant resolution of the intended value.

In section 2, we will explain the structure of the ADC-Assisted GRO TDC with digital calibration. In section 3, we will explain the structure and operation of the sub-block and the procedure of the digital calibration. And the layout and simulation results will be shown in section 4.

II. PROPOSED ARCHITECTURE

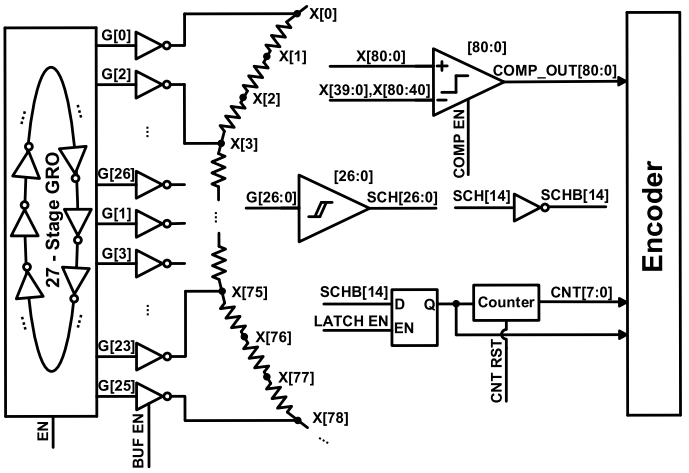

Fig. 1. Block diagram of the porposed TDC

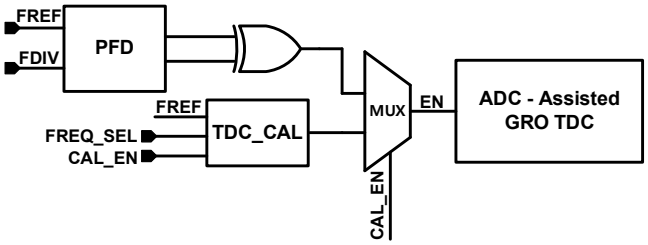

Fig. 2. Top block diagram of the porposed TDC for Calibration

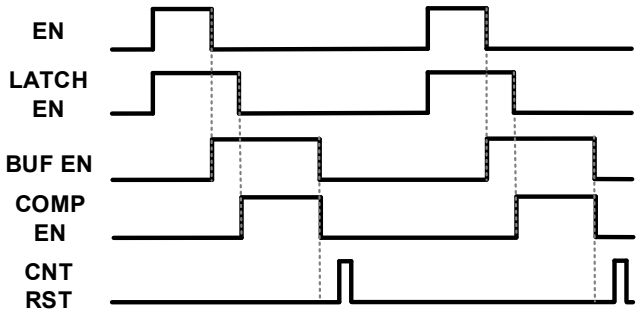

Fig. 3. Timing diaram of the enable signals

The top block diagram of the ADC-Assisted GRO TDC proposed in this paper is shown in figure 1. Basically, a 27-stage multi-stage GRO cell was designed to obtain a high resolution of 12 ps. In addition, simple Flash ADC with a resistive interpolator is used to make a resolution three times higher of 4 ps. Coarse output can be obtained by applying one of the GRO node as an input of the Schmitt trigger and counting the output using counter. Fine output can be obtained by checking the amount of change in the output code of Flash ADC. The output of the counter and the Flash ADC enter the encoder, and the final output result reflecting each resolution is calculated. Encoder also includes an averaging option, so higher resolution can be implemented as needed.

Next, the path configured for digital calibration is shown in figure 2. When the S<1> signal is high, the signal from TDC_CAL cell is applied as the enable signal of the ADC-Assisted GRO TDC cell to calculate the output at that time. In TDC_CAL cell, the input clock is 50 MHz clock, and two signals which the frequency is divided by two and four are generated. The output codes when these signals are received as an enable signals are calculated, and the gain and offset of the currently operating TDC are identified through this. Then the subsequent output is calculated by reflecting this gain and offset.

The GRO TDC in this paper operates according to the timing diagram in Figure 3. When an EN signal generated by PFD or TDC_CAL cell comes in, internal enable signals for latch, comparator, buffer, and CNT are generated. To ensure that the oscillation of the GRO cell is well transmitted through the latch to the CNT, the latch EN turns on at the same time as the EN signal and turns off after EN signal turns off. How long it will be turned on can be changed by adjusting the control bit. The buffer turns on after the EN signal is turned off, and the comparator turns on when the latch EN is turned off, allowing a stable voltage to enter the input of the comparator. The comparator turns off after a sufficient time to operate, and the time can be changed by adjusting the control bit. When the comparator is turned off, the buffer is turned off as well. Finally, CNT is generated by a certain time after all other enable signals are turned off, allowing it to count again in the next cycle.

III. Building Blocks

A. GRO TDC with Multi-Path Delay Cell

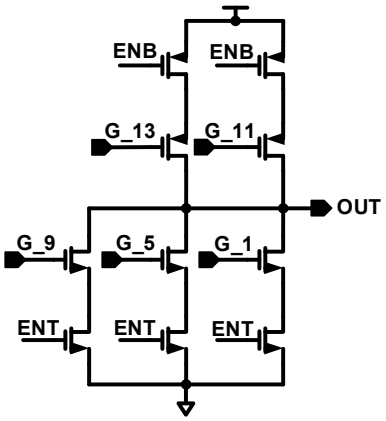

Fig. 4. Multi-path delay cell

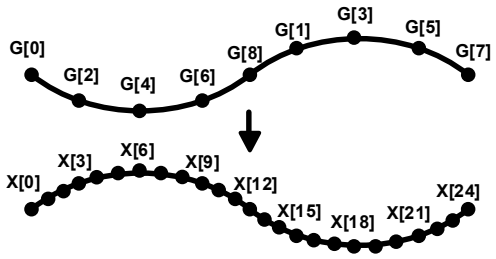

Fig. 5. Operation of the resistive interpolator

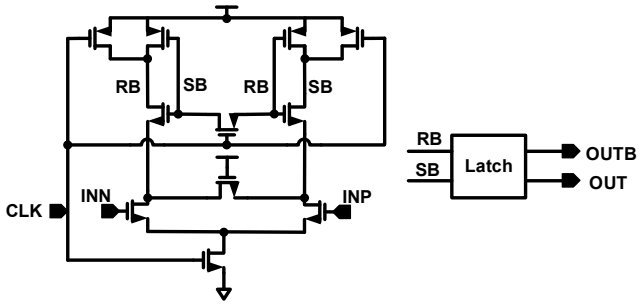

Fig. 6. Schematic of the Comparator

In order to overcome the limitations of delay of one inverter in this process, a GRO TDC based on a multi-path delay cell was designed to improve the resolution. The schematic of multi-path delay cell is shown in figure 4. To achieve the intended resolution of 12 ps, a delay cell with 5 multi-path inputs was used, and the GRO consisted of 27 delay cells. It is designed to prevent errors by reducing the mismatch on the layout as much as possible.

B. Flash ADC with Resistive Interpolator

A flash ADC with a resistive-interpolator was used to obtain a higher resolution than the resolution of the GRO TDC itself. Figure 5 shows the GRO output voltages and Flash ADC output for 8-stage GRO case. Like in figure 4, inserting three resistors between each node makes voltages three times denser. So the resolution can be three times higher than the resolution of GRO TDC itself. Figure 6 is the schematic of the comparator used in Flash-ADC. Basic differential ADC is used in this paper.

C. TDC Encoder

The TDC in this paper calculates the output results through the encoder. This encoder has an option to improve the resolution of the output through averaging.

The basic operation of the encoder is performed in the following process. The result that reflects the resolution difference between the counter output code and the comparator output code is calculated. The comparator output code reflected as the difference of the previous output code and the current output code. The counter output code is reflected according to the state of the latch, and the amount of change of the comparator output code whether it is more than half or not. Final, an integral output code of 14 bits and a fractional output code of 3 bits are generated.

GRO cell in the GRO TDC in this paper operates in a way that maintains the previous oscillation state and then oscillates

again form that state, so averaging the output can increases the resolution. In this case, it is possible to calculate the averaging result up to 8 times as an output.

D. Digital Calibration

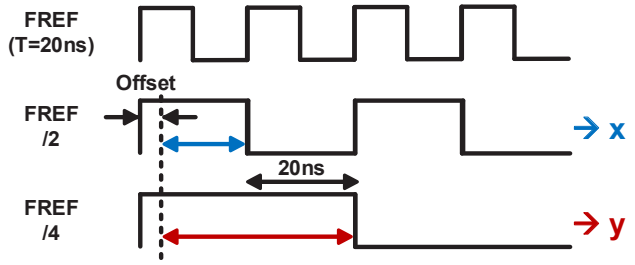

Fig. 7. Timing diagram for the digital calibration

TDC in this paper can have a constant resolution through digital calibration. Timing diagram for the digital calibration is shown in figure 7. Calibration is performed using a signal that the frequency is divided into two and divided into four of a 50 MHz input signal. The overall method is to check the offset and gain of the operating TDC, and then to enable an output reflecting that offset and gain in the subsequent result.

First, the output code using the signal that the frequency is divided by two as the TDC enable signal is calculated. And then, the output using the signal that the frequency is divided by four as the TDC enable signal is also calculated. If the two results are x and y, respectively, then if x is subtracted from y, the offset is canceled. So that the output code that the TDC operated for a complete 20 ns can be confirmed. Through this, it is possible to check the gain of the currently operating TDC. In addition, the offset of the TDC can be confirmed by comparing the value of x with the value of x subtracted from y.

The gain and offset values of the TDC calculated through this process are reflected in the subsequent output code. So the same resolution can be secured even if the resolution of GRO is changed due to some corner variation.

IV. Experimental Results

A. Layout

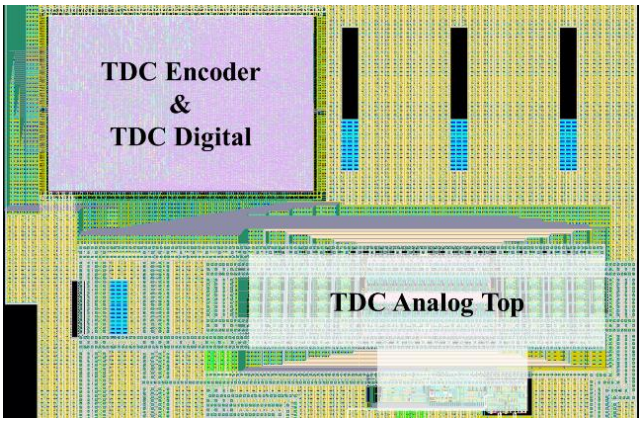

Fig. 8. Top layout of the proposed TDC

Figure 8 is the top layout of TDC proposed in this paper. It is designed with 130nm CMOS Process. The area of the digital top with TDC encoder is 416.8 μm × 275.6 μm, and the area of the TDC Analog Top is 558.5 μm × 243.5 μm.

B. Simulation Results

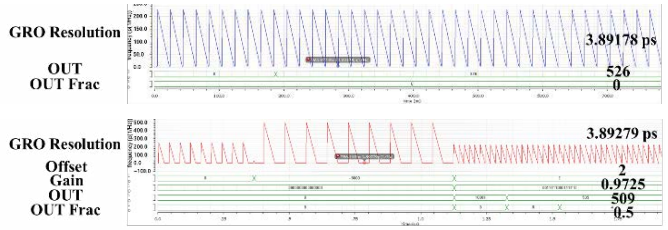

Fig. 9. Simulation Results for TT / 40 °C case

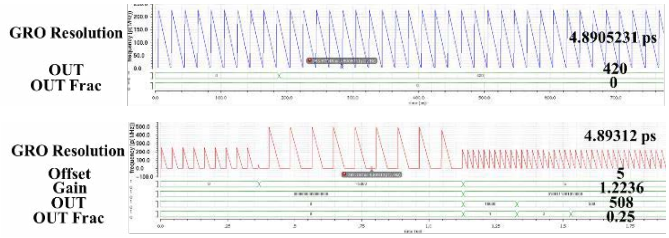

Fig. 10. Simulation Results for SS / 85 °C case

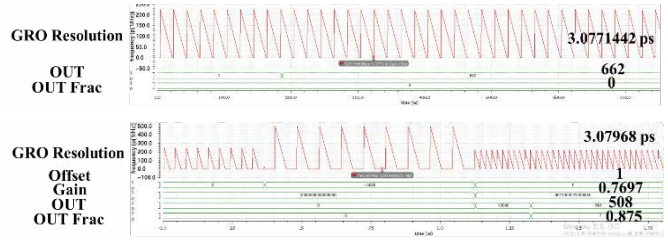

Fig. 11. Simulation Results for FF / -40 °C case

TABLE I. Simulation Results of TDC

Process / Temperature	*Resolution*	Output Code	
		W/O Calibration	*W/ Calibration*
TT / 40 °C	3.89 ps	526	509.5
SS / 85 °C	4.89 ps	420	508.25
FF / -40 °C	3.08 ps	662	508.875

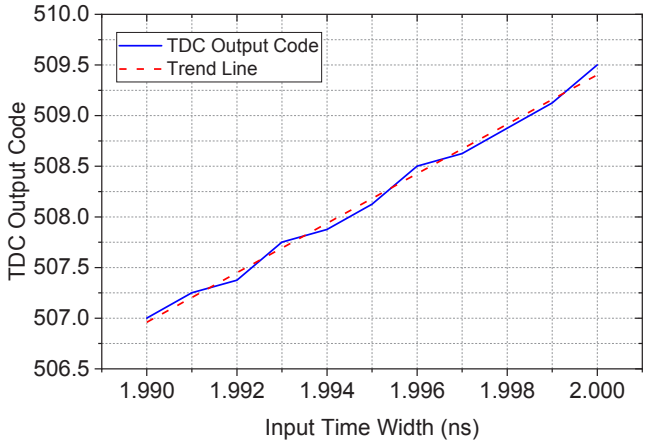

Fig. 12. TDC output code according to the input time width

Figure 9, 10, 11 is the simulation results of the TDC in this paper for some corner cases when the enable time is 2 ns. The input is 2 ns, and the intended resolution is 4 ps, so the ideal output code is 500. This is the result of comparing the output when it is not in calibration mode and when it is in calibration mode for three corner cases. The table summarizes this is shown in table 1.

It can be seen that there is an error of about 8 between the ideal code and the calibrated code. There is PFD in the actual operation path, but there is no PFD in the path for calibration. This is the reason of the error, so it can be solved simply by adding PFD to the calibration path.

Figure 12 is the simulation result of the TDC output code according to the input time width. When checking the TDC output by increasing the input time width by 1 ps, it is confirmed that the output code increases proportionally. So, it shows that this TDC has linearity.

V. Conclusion

This paper proposes the structure of ADC-Assisted GRO TDC with digital calibration. The TDC has a high resolution through the use of ADC-Assisted structures, multi-path delay cells, and averaging in encoder. And it has a constant resolution through digital calibration. A high resolution can ensure good performance when applied to multiple systems, and a constant resolution allows the entire system to be stable from PVT variation. The GRO TDC in this paper is designed with a 130 nm CMOS process, and if the process changes, the desired resolution can be easily obtained by changing the number of GRO stages, the number of multi-inputs of multi-path delay cells, and the number of resistors in the resistive interpolators.

Acknowledgment

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