Dual-Pole 4-Channel Receive Beamforming IC for Ka-band Satellite Communication

Junhan Lim
Satellite Payload Research Section
ETRI
Daejeon, South Korea
flawnsgks@etri.re.kr

Seong-Mo Moon
Satellite Payload Research Section
ETRI
Daejeon, South Korea
smmoon@etri.re.kr

Dong-Pil Chang
Satellite Payload Research Section
ETRI
Daejeon, South Korea
dpjang@etri.re.kr

Byoung-Sun Lee
Satellite Payload Research Section
ETRI
Daejeon, South Korea
lbs@etri.re.kr

Jin-Seok Park
Department of ICT Convergence
System Engineering
Chonnam National University
Gwangju, South Korea
jinseok131@jnu.ac.kr

Abstract— This abstract outlines the presentation of a dual-pole 4-channel receive beamforming integrated chip (IC) for Ka-band satellite communication. The chip features a variable gain phase shifter constructed around a vector summation type phase shifter. Additionally, the IC includes a specially designed digital-to-analogue converter (DAC) for current steering with an I/Q generator utilizing an RC–LR polyphase filter to minimize insertion loss. Circuit techniques are presented to have higher performance with smaller chip size, and lower power consumption. Orthogonal phase and gain control in a single block are firstly achieved using the proposed dual-vector synthesis technique, which greatly reduces chip size and power consumption. It has 30 dB gain dynamic range and 6-bit phase control step all over 360°. For combining the 8 different channels into a single stream, highly optimized 4:1 and 2:1 combiners are adapted. It shows a measured RMS phase error of 1.6° and RMS amplitude error of 0.15 dB over 18 – 21 GHz, while 15 dB gain varying and 360° phase shifting. It has 27 dB coherent gain and 2.9 dB coherent Noise Figure. The proposed dual pole 4-CH beamforming IC was implemented in a 0.18-um SiGe BiCMOS technology with the chip size of 3.8 mm x 3.0 mm. A single channel consumes about 33 mA on 3.3 V supply voltage.

Keywords—phased array system, beamforming, variable gain amplifier, phase shifter, satellite communication

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