

# A 130–147.7 GHz CMOS Low Noise Amplifier for Satellite Communication

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**Abstract**—This study proposes a three-stage low-noise amplifier (LNA) for D-band satellite communication, where each stage has a different topology. Each stage is configured using a single-ended common-source (CS), a single-ended cascode, and a differential cascode structure to reduce the noise figure while ensuring sufficient gain and linearity. To reduce the noise figure, a large transistor technique is applied to the first stage, while the capacitive neutralization technique is applied to the third stage to enhance gain. To verify this development, a proposed LNA was implemented using 60-nm bulk CMOS technology. The core size of this LNA is 0.086 mm<sup>2</sup>. Measurement results show that 16.77 dB peak gain, 6.42–7.02 dB NF. The LNA has an input 1-dB compression point (IP1dB) of -15 dBm at 130-150 GHz and the power consumption is 60 mW.

*Keywords*—CMOS, D-band, Low noise amplifier, Satellite communication

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